AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of operating a cache in a computer system, the cache storing items associated with addresses in memory in the computer system, the cache having at least one way with a tag array and a data array, with information in the tag array indicating, for ~~each~~ an address in memory applied to the cache, whether information in the data array is associated with the applied address ~~in memory~~, with the data array implemented as an array of cells connected to lines and a plurality of sense amps, with a sense amp being connectable to each of the lines, comprising, for each of the at least one way:

a) making a determination, based on information stored in the tag array, whether an item associated with the applied address is stored in the way in the data array;

b) selectively altering the state of at least one line in the way in the data array, that at least one line being associated with the applied address, the selective altering placing each of the at least one line in a state based on a value stored in at least one cell of the way of the data array at the applied address and the selective altering starting before completing the determination; and

c) after completing the determination, when the information indicates an item is stored in the way in the data array, selectively enabling at least one sense amp associated with [[a]] the at least one line in the way in the data array when it is determined that an item associated with the applied address is stored in the way.

2. (Original) The method of claim 1 wherein each sense amp is connectable to a plurality of lines and enabling the sense amp associated with a line in the indicated way comprises connecting the sense amp to a single one of the plurality of lines selectively in response to the information read from the tag array.

3. (Original) The method of claim 1 additionally comprising providing as a bit in the output of the cache, the output of the sense amp.

4. (Original) The method of claim 3 wherein the data array is implemented as memory having a plurality of banks, with each applied address associated with one or more lines in one of the banks and not associated with lines in at least a portion of the plurality of banks, the method further comprising, between the time that an address is applied to the tag array and an output is provided from the sense amp, performing a memory operation in a bank in the portion of the plurality of banks.

5. (Original) The method of claim 1 wherein the at least one way comprises 2 ways.

6. (Original) The method of claim 5 wherein the at least one way consists of 4 ways.

7. (Original) The method of claim 1 wherein making a determination comprises for each way in the cache: reading a tag field from a location in the tag array and comparing the value in the tag field to a portion of the bits in the applied address.

8. (Original) The method of claim 7 additionally comprising controlling the charge on each of the plurality of lines in the data array to place the lines in a predetermined state before starting to alter the state of the line.

9. (Original) The method of claim 1 wherein each of the lines comprises a column line in the memory and altering the state of at least one line comprises asserting a word line in the memory.

10-21. Canceled

22. (Currently Amended) A method of operating a cache in a computer system, the cache storing items associated with addresses in memory in the computer system, the cache having a tag array and a data array, the data array having a plurality of ways with information in the tag array indicating, for each address applied to the cache, in which, if any, way in the data array information associated with the applied address is stored, with the data array implemented as arrays of cells

connected to lines and plurality of sense amps, with a sense amp being connectable to each of the ~~word~~ lines,

a) applying a first portion of the applied address to the tag array to address a location in each way of the tag array;

b) comparing a second portion of the applied address to information read from the addressed locations in each way of the tag array to produce at a first time, an indication of a match between the first input and one of the ways;

c) before the first time, altering the state of lines associated with the first portion of the applied address in each way of the data array, with the state of the lines based on information stored in the data array; and

d) after the first time, sensing the state of a line associated with the first portion of the applied address in the data array, with the sensed line selected in response to the ~~output of the comparator~~ indication of a match.

23. (Original) The method of operating a cache in a computer system of claim 22 wherein each of the lines comprises a bit line in a semiconductor memory.

24. (Currently Amended) The method of operating a cache in a computer system of claim 23 wherein altering the state of lines comprises activating, for each of the lines, a cell connected to a word line in the
semiconductor memory.

25. (Original) The method of operating a cache in a computer system of claim 22 additionally comprising placing the lines in a predetermined charge state.

26. (Original) The method of operating a cache in a computer system of claim 25 wherein altering the state of the lines comprises altering the charge on each line based on information stored in one memory cell.

27. (Original) The method of operating a cache in a computer system of claim 26 wherein each of the lines comprises a differential pair and altering the charge on the line comprises altering the charge difference between the lines.

28. (Original) The method of claim 22 wherein sensing the state of a line comprises enabling a sense amp selected based on the indication of a match.

29. (Original) The method of claim 22 wherein sensing the state of a line comprises activating a multiplexer based on the indication of a match to connect a selected line to a sense amp.

30. (New) The method of claim 1 wherein, selectively enabling the sense amp comprises not enabling the sense amp during a cache read operation when it is determined that no item associated the applied address is stored in the way.

31. (New) The method of claim 1 wherein, selectively altering the state of at least one line in the way in the data array occurs concurrently with making the determination.

32. (New) A method of performing a read operation with a cache in a computer system, the cache storing items associated with addresses in memory in the computer system, the cache having at least one way with a tag array and a data array, with information in the tag array indicating, for an address in memory applied to the cache, whether information in the data array is associated with the applied address, with the data array comprising a plurality of cells connected to a line and a sense amp connectable to the line, the method comprising:

a) during a first interval:

i) accessing a value the tag array based on the applied address;

ii) selecting a cell in the data array based on the applied address;

iii) altering the state of the line by connecting the selected cell to the line; and

iv) making a determination, based on the accessed value, whether an item associated with the applied address is stored in the way in the data array; and

b) during a second interval, the second interval occurring after the first interval, in response to a determination that an item associated with the applied address is stored in the way in the data array, selectively enabling the sense amp.

33. (New) The method of claim 32, further comprising, during the second interval, in response to a determination that an item associated with the applied address is not stored in the way in the data array, indicating a cache miss.

34. (New) The method of claim 32, further comprising, during the first interval, precharging the line.

addresses from which data in the data array has been copied. With this architecture, reading information from the cache is generally a two-phase operation. When a memory address is applied to a cache, the first phase involves determining, based on information in the tag array, whether a copy of the information from the applied memory address is stored in the cache. The second phase involves accessing the information from the data array, if it is stored in the cache.

The present application describes known alternative approaches to performing these two phases. FIG. 6 illustrates that the two phases may be performed sequentially, in subsequent intervals indicated as intervals 510 and 512. If the read from the tag array that occurs as part of the first phase indicates that no copy of the requested information is stored in the cache, the second phase is not performed.

FIG. 5 illustrates an alternative in which the phases are performed in parallel. Parallel operation as illustrated in FIG. 5 takes advantage of an organization of a cache memory in which specific memory address correspond to specific cache locations. Because of this organization, it is possible to identify the location in the cache at which data for a particular memory address would be stored, if a copy of that data is stored in the cache. However, it cannot be known until the tag array is read whether a copy of the required data is actually stored in that location. Accordingly, to perform the two phases in parallel, information may be read from the tag array and the data array in parallel when a memory address is applied to the cache. Based on the information read from the tag array, a determination is made whether the data read from the data array represents the desired information. Based on this determination, either the information read from the data array is output from the cache or the cache outputs an indication that the information is not stored in the cache.

While the invention relates to a cache with a tag array and a data array that store the same types of information as in the prior art, the present application describes a sequence of events in accessing the data array that is different than either of the prior art approaches. As described in paragraph 59 of the published application, the Applicant has appreciated that a different timing sequence for accessing the data array allows fast and low power access to the cache, which is